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**EE 4550L**

**IC Hardware Security and Trust LAB**

**SPRING 2024**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 14th February 2024**

**Report due date: 16th February 2024**

1. **OBJECTIVE**

To learn how to use Synopsys TetraMax for automatic test pattern generation.

1. **PROCEDURE**

Load the required netlists as library modules, then load the main netlist you want to test as not a library module. Then build the circuit by pressing the build button on the main screen and then the run button on the pop-up screen. Then run a DRC by pressing the DRC button on the main screen then the run button on the pop-up screen. Then generate the test report by clicking ATPG, select “add all faults” on the pop-up screen and click auto. Finally, save the report to a file by clicking Write Pat. On the main screen, select “STIL99” as the file format on the pop-up screen and click browse to select where to save the report. Repeat all steps for all netlists to test.

1. **RESULT**

|  |
| --- |
| STIL 1.0;  Header {  Title " TetraMAX(R) V-2023.12-i20231127\_013657 STIL output";  Date "Thu Feb 8 18:54:57 2024";  History {  Ann {\* Uncollapsed Stuck Fault Summary Report \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* fault class code #faults \*}  Ann {\* ------------------------------ ---- --------- \*}  Ann {\* Detected DT 10 \*}  Ann {\* Possibly detected PT 0 \*}  Ann {\* Undetectable UD 0 \*}  Ann {\* ATPG untestable AU 0 \*}  Ann {\* Not detected ND 0 \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* total faults 10 \*}  Ann {\* test coverage 100.00% \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* \*}  Ann {\* Pattern Summary Report \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* #internal patterns 3 \*}  Ann {\* #basic\_scan patterns 3 \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* \*}  Ann {\* There are no rule fails \*}  Ann {\* There are no clocks \*}  Ann {\* There are no constraint ports \*}  Ann {\* There are no equivalent pins \*}  Ann {\* There are no net connections \*}  Ann {\* top\_module\_name = OneBitFullAdder \*}  Ann {\* Unified STIL Flow \*}  Ann {\* min\_n\_shifts = 1 \*}  Ann {\* serial\_flag = 1 \*}  Ann {\* PSDF = NO\_PSD\_FILE \*}  Ann {\* PSDS = 0 \*}  Ann {\* PSDA = #3#0#0/0 \*}  }  }  Signals {  "A" In; "B" In; "Cin" In; "S" Out; "Cout" Out;  }  SignalGroups {  "\_default\_In\_Timing\_" = '"A" + "B" + "Cin"'; // #signals=3  "\_pi" = '"A" + "B" + "Cin"'; // #signals=3  "\_in" = '"A" + "B" + "Cin"'; // #signals=3  "\_default\_Out\_Timing\_" = '"S" + "Cout"'; // #signals=2  "\_po" = '"S" + "Cout"'; // #signals=2  "\_out" = '"S" + "Cout"'; // #signals=2  }  Timing {  WaveformTable "\_default\_WFT\_" {  Period '100ns';  Waveforms {  "\_default\_In\_Timing\_" { 0 { '0ns' D; } }  "\_default\_In\_Timing\_" { 1 { '0ns' U; } }  "\_default\_In\_Timing\_" { Z { '0ns' Z; } }  "\_default\_In\_Timing\_" { N { '0ns' N; } }  "\_default\_Out\_Timing\_" { X { '0ns' X; } }  "\_default\_Out\_Timing\_" { H { '0ns' X; '40ns' H; } }  "\_default\_Out\_Timing\_" { T { '0ns' X; '40ns' T; } }  "\_default\_Out\_Timing\_" { L { '0ns' X; '40ns' L; } }  }  }  }  UserKeywords ScanChainGroups;  ScanStructures {  // Uncomment and modify the following to suit your design  // ScanChain "chain\_name" { ScanIn "chain\_input\_name"; ScanOut "chain\_output\_name"; }  }  PatternBurst "\_burst\_" {  PatList { "\_pattern\_" {  }  }}  PatternExec {  PatternBurst "\_burst\_";  }  UserKeywords ActiveScanChains;  Procedures {  "capture" {  W "\_default\_WFT\_";  C { "\_po"=XX; }  "forcePI": V { "\_pi"=###; }  "measurePO": V { "\_po"=##; }  }  // Uncomment and modify the following to suit your design  // load\_unload {  // V { } // force clocks off and scan enable pins active  // Shift { V { \_si=#; \_so=#; }} // pulse shift clocks  // }  }  MacroDefs {  }  Pattern "\_pattern\_" {  W "\_default\_WFT\_";  "precondition all Signals": C { "\_pi"=000; "\_po"=XX; }  "pattern 0": Call "capture" {  "\_pi"=100; "\_po"=HL; }  "pattern 1": Call "capture" {  "\_pi"=001; "\_po"=HL; }  "pattern 2": Call "capture" {  "\_pi"=011; "\_po"=LH; }  }  // Patterns reference 6 V statements, generating 6 test cycles |

Uncollapsed Stuck Fault Summary Report for the adder.

|  |
| --- |
| STIL 1.0;  Header {  Title " TetraMAX(R) V-2023.12-i20231127\_013657 STIL output";  Date "Thu Feb 8 19:06:36 2024";  History {  Ann {\* Uncollapsed Stuck Fault Summary Report \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* fault class code #faults \*}  Ann {\* ------------------------------ ---- --------- \*}  Ann {\* Detected DT 68 \*}  Ann {\* Possibly detected PT 0 \*}  Ann {\* Undetectable UD 0 \*}  Ann {\* ATPG untestable AU 0 \*}  Ann {\* Not detected ND 0 \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* total faults 68 \*}  Ann {\* test coverage 100.00% \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* \*}  Ann {\* Pattern Summary Report \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* #internal patterns 4 \*}  Ann {\* #basic\_scan patterns 4 \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* \*}  Ann {\* rule severity #fails description \*}  Ann {\* ---- -------- ------ --------------------------------- \*}  Ann {\* N1 fatal 1 parsing error \*}  Ann {\* N5 warning 1 redefined module \*}  Ann {\* \*}  Ann {\* There are no clocks \*}  Ann {\* There are no constraint ports \*}  Ann {\* There are no equivalent pins \*}  Ann {\* There are no net connections \*}  Ann {\* top\_module\_name = FourBitFullAdder \*}  Ann {\* Unified STIL Flow \*}  Ann {\* min\_n\_shifts = 1 \*}  Ann {\* serial\_flag = 1 \*}  Ann {\* PSDF = NO\_PSD\_FILE \*}  Ann {\* PSDS = 0 \*}  Ann {\* PSDA = #4#0#0/0 \*}  }  }  Signals {  "A(4)" In; "A(3)" In; "A(2)" In; "A(1)" In; "B(4)" In; "B(3)" In; "B(2)" In; "B(1)" In;  "Cin" In; "Cout" Out; "S(4)" Out; "S(3)" Out; "S(2)" Out; "S(1)" Out;  }  SignalGroups {  "\_default\_In\_Timing\_" = '"A(4)" + "A(3)" + "A(2)" + "A(1)" + "B(4)" + "B(3)" + "B(2)"  + "B(1)" + "Cin"'; // #signals=9  "\_pi" = '"A(4)" + "A(3)" + "A(2)" + "A(1)" + "B(4)" + "B(3)" + "B(2)" + "B(1)"  + "Cin"'; // #signals=9  "\_in" = '"A(4)" + "A(3)" + "A(2)" + "A(1)" + "B(4)" + "B(3)" + "B(2)" + "B(1)"  + "Cin"'; // #signals=9  "\_default\_Out\_Timing\_" = '"Cout" + "S(4)" + "S(3)" + "S(2)" + "S(1)"'; // #signals=5  "\_po" = '"Cout" + "S(4)" + "S(3)" + "S(2)" + "S(1)"'; // #signals=5  "\_out" = '"Cout" + "S(4)" + "S(3)" + "S(2)" + "S(1)"'; // #signals=5  }  Timing {  WaveformTable "\_default\_WFT\_" {  Period '100ns';  Waveforms {  "\_default\_In\_Timing\_" { 0 { '0ns' D; } }  "\_default\_In\_Timing\_" { 1 { '0ns' U; } }  "\_default\_In\_Timing\_" { Z { '0ns' Z; } }  "\_default\_In\_Timing\_" { N { '0ns' N; } }  "\_default\_Out\_Timing\_" { X { '0ns' X; } }  "\_default\_Out\_Timing\_" { H { '0ns' X; '40ns' H; } }  "\_default\_Out\_Timing\_" { T { '0ns' X; '40ns' T; } }  "\_default\_Out\_Timing\_" { L { '0ns' X; '40ns' L; } }  }  }  }  UserKeywords ScanChainGroups;  ScanStructures {  // Uncomment and modify the following to suit your design  // ScanChain "chain\_name" { ScanIn "chain\_input\_name"; ScanOut "chain\_output\_name"; }  }  PatternBurst "\_burst\_" {  PatList { "\_pattern\_" {  }  }}  PatternExec {  PatternBurst "\_burst\_";  }  UserKeywords ActiveScanChains;  Procedures {  "capture" {  W "\_default\_WFT\_";  C { "\_po"=XXXXX; }  "forcePI": V { "\_pi"=\r9 # ; }  "measurePO": V { "\_po"=#####; }  }  // Uncomment and modify the following to suit your design  // load\_unload {  // V { } // force clocks off and scan enable pins active  // Shift { V { \_si=#; \_so=#; }} // pulse shift clocks  // }  }  MacroDefs {  }  Pattern "\_pattern\_" {  W "\_default\_WFT\_";  "precondition all Signals": C { "\_pi"=\r9 0 ; "\_po"=XXXXX; }  "pattern 0": Call "capture" {  "\_pi"=111101111; "\_po"=HLHHH; }  "pattern 1": Call "capture" {  "\_pi"=000011110; "\_po"=LHHHH; }  "pattern 2": Call "capture" {  "\_pi"=000010001; "\_po"=LHLLH; }  "pattern 3": Call "capture" {  "\_pi"=111011000; "\_po"=HHLHL; }  }  // Patterns reference 8 V statements, generating 8 test cycles |

Uncollapsed Stuck Fault Summary Report for the 4 bit adder.

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| --- |
| STIL 1.0;  Header {  Title " TetraMAX(R) V-2023.12-i20231127\_013657 STIL output";  Date "Thu Feb 8 19:30:27 2024";  History {  Ann {\* Uncollapsed Stuck Fault Summary Report \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* fault class code #faults \*}  Ann {\* ------------------------------ ---- --------- \*}  Ann {\* Detected DT 92 \*}  Ann {\* Possibly detected PT 0 \*}  Ann {\* Undetectable UD 0 \*}  Ann {\* ATPG untestable AU 0 \*}  Ann {\* Not detected ND 0 \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* total faults 92 \*}  Ann {\* test coverage 100.00% \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* \*}  Ann {\* Pattern Summary Report \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* #internal patterns 3 \*}  Ann {\* #basic\_scan patterns 3 \*}  Ann {\* ----------------------------------------------- \*}  Ann {\* \*}  Ann {\* rule severity #fails description \*}  Ann {\* ---- -------- ------ --------------------------------- \*}  Ann {\* N1 fatal 4 parsing error \*}  Ann {\* N5 warning 2 redefined module \*}  Ann {\* N8 fatal 2 invalid construct \*}  Ann {\* \*}  Ann {\* There are no clocks \*}  Ann {\* There are no constraint ports \*}  Ann {\* There are no equivalent pins \*}  Ann {\* There are no net connections \*}  Ann {\* top\_module\_name = FourBitAddSub \*}  Ann {\* Unified STIL Flow \*}  Ann {\* min\_n\_shifts = 1 \*}  Ann {\* serial\_flag = 1 \*}  Ann {\* PSDF = NO\_PSD\_FILE \*}  Ann {\* PSDS = 0 \*}  Ann {\* PSDA = #3#0#0/0 \*}  }  }  Signals {  "a(4)" In; "a(3)" In; "a(2)" In; "a(1)" In; "b(4)" In; "b(3)" In; "b(2)" In; "b(1)" In;  "m" In; "s(4)" Out; "s(3)" Out; "s(2)" Out; "s(1)" Out; "cout" Out;  }  SignalGroups {  "\_default\_In\_Timing\_" = '"a(4)" + "a(3)" + "a(2)" + "a(1)" + "b(4)" + "b(3)" + "b(2)"  + "b(1)" + "m"'; // #signals=9  "\_pi" = '"a(4)" + "a(3)" + "a(2)" + "a(1)" + "b(4)" + "b(3)" + "b(2)" + "b(1)"  + "m"'; // #signals=9  "\_in" = '"a(4)" + "a(3)" + "a(2)" + "a(1)" + "b(4)" + "b(3)" + "b(2)" + "b(1)"  + "m"'; // #signals=9  "\_default\_Out\_Timing\_" = '"s(4)" + "s(3)" + "s(2)" + "s(1)" + "cout"'; // #signals=5  "\_po" = '"s(4)" + "s(3)" + "s(2)" + "s(1)" + "cout"'; // #signals=5  "\_out" = '"s(4)" + "s(3)" + "s(2)" + "s(1)" + "cout"'; // #signals=5  }  Timing {  WaveformTable "\_default\_WFT\_" {  Period '100ns';  Waveforms {  "\_default\_In\_Timing\_" { 0 { '0ns' D; } }  "\_default\_In\_Timing\_" { 1 { '0ns' U; } }  "\_default\_In\_Timing\_" { Z { '0ns' Z; } }  "\_default\_In\_Timing\_" { N { '0ns' N; } }  "\_default\_Out\_Timing\_" { X { '0ns' X; } }  "\_default\_Out\_Timing\_" { H { '0ns' X; '40ns' H; } }  "\_default\_Out\_Timing\_" { T { '0ns' X; '40ns' T; } }  "\_default\_Out\_Timing\_" { L { '0ns' X; '40ns' L; } }  }  }  }  UserKeywords ScanChainGroups;  ScanStructures {  // Uncomment and modify the following to suit your design  // ScanChain "chain\_name" { ScanIn "chain\_input\_name"; ScanOut "chain\_output\_name"; }  }  PatternBurst "\_burst\_" {  PatList { "\_pattern\_" {  }  }}  PatternExec {  PatternBurst "\_burst\_";  }  UserKeywords ActiveScanChains;  Procedures {  "capture" {  W "\_default\_WFT\_";  C { "\_po"=XXXXX; }  "forcePI": V { "\_pi"=\r9 # ; }  "measurePO": V { "\_po"=#####; }  }  // Uncomment and modify the following to suit your design  // load\_unload {  // V { } // force clocks off and scan enable pins active  // Shift { V { \_si=#; \_so=#; }} // pulse shift clocks  // }  }  MacroDefs {  }  Pattern "\_pattern\_" {  W "\_default\_WFT\_";  "precondition all Signals": C { "\_pi"=\r9 0 ; "\_po"=XXXXX; }  "pattern 0": Call "capture" {  "\_pi"=100111110; "\_po"=HLLLH; }  "pattern 1": Call "capture" {  "\_pi"=001001011; "\_po"=HHLHL; }  "pattern 2": Call "capture" {  "\_pi"=011100000; "\_po"=LHHHL; }  }  // Patterns reference 6 V statements, generating 6 test cycles |

Uncollapsed Stuck Fault Summary Report for the 4 bit adder/subtractor.

A table with numbers and symbols

Description automatically generated

Table listing the number of faults, test patterns, fault coverage, and number of undetectable faults for each circuit described in VHDL.

1. **CONCLUSION**

My results satisfy the requirements. I do not believe that it is possible to improve my design with better results as there was no designing and only running a previous design through an automatic test pattern generator to test for faults. I have learned how to use Synopsys TetraMax from this lab.